Amendments to the Claims:

Please cancel claims 8 and 21 as follows. Please amend claims 1 and 14 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A method of fabricating a semiconductor device comprising:

providing a passivation layer on a circuit element of the semiconductor device;

patterning the passivation layer to expose an upper surface of the circuit element;

providing a photosensitive layer on the passivation layer and the circuit element;

providing a photoresist layer on the photosensitive layer, wherein the photoresist layer is of a thickness that is sufficient to prevent the underlying photo-sensitive layer from becoming exposed during the exposing step, and is of a thickness so as to be fully removed during the removing step;

exposing a region of the photoresist layer and the photosensitive layer above the circuit element; and

removing the photoresist layer and the exposed region of the photosensitive layer.

2. (original) The method of claim 1 wherein providing the passivation layer comprises a stacked CVD oxide layer and CVD nitride layer.

3. (original) The method of claim 1 wherein patterning the passivation layer comprises selectively etching the passivation layer to expose the circuit element.

4. (original) The method of claim 1 further comprising:

providing a dielectric layer on a semiconductor substrate; and

providing the circuit element on the dielectric layer.

5. (original) The method of claim 1 wherein the circuit element comprises a conductive element.

6. (original) The method of claim 5 wherein the conductive element comprises an element selected from the group consisting of: a bonding pad, a fuse, a scribe lane, a metal layer, and a device terminal.

7. (original) The method of claim 1 wherein the photosensitive layer comprises one of: a polyimide layer, a novolak layer, and a resol layer.

8. (canceled)

9. (original) The method of claim 1 wherein the photoresist layer is of a thickness less than or equal to about 500 Å.

10. (original) The method of claim 1 wherein removing the photoresist layer and the exposed region of the photosensitive layer comprises developing the photoresist layer and the exposed region with a developer.

11. (original) The method of claim 10 wherein the developer comprises tetra-methyl-ammonium-hydroxide (TMAH).

12. (original) The method of claim 11 wherein the developer removes the photoresist layer and the exposed region of the photosensitive layer contemporaneously.

13. (original) The method of claim 1 wherein the photoresist layer protects regions of the photosensitive layer, other than the region above the circuit element, from exposure during the exposing step.

14. (currently amended) A semiconductor device prepared in accordance with the steps of:
providing a passivation layer on a circuit element of a semiconductor device;

patterning the passivation layer to expose an upper surface of the circuit element;

providing a photosensitive layer on the passivation layer and the circuit element;

providing a photoresist layer on the photosensitive layer, wherein the photoresist layer is of a thickness that is sufficient to prevent the underlying photo-sensitive layer from becoming exposed during the exposing step, and is of a thickness so as to be fully removed during the removing step;

exposing a region of the photoresist layer and the photosensitive layer above the circuit element; and

removing the photoresist layer and the exposed region of the photosensitive layer.

15. (original) The semiconductor device of claim 14 wherein providing the passivation layer comprises a stacked CVD oxide layer and CVD nitride layer.

16. (original) The semiconductor device of claim 14 wherein patterning the passivation layer comprises selectively etching the passivation layer to expose the circuit element.

17. (original) The semiconductor device of claim 14 further comprising:

providing a dielectric layer on a semiconductor substrate; and

providing the circuit element on the dielectric layer.

18. (original) The semiconductor device of claim 14 wherein the circuit element comprises a conductive element.

19. (original) The semiconductor device of claim 18 wherein the conductive element comprises an element selected from the group consisting of: a bonding pad, a fuse, a scribe lane, a metal layer, and a device terminal.

20. (original) The semiconductor device of claim 14 wherein the photosensitive layer comprises one of: a polyimide layer, a novolak layer, and a resol layer.

21. (original) The semiconductor device of claim 14 wherein providing a photoresist layer on the photosensitive layer comprises providing a photoresist layer of a thickness that is sufficient to prevent the underlying photo-sensitive layer from becoming exposed during the exposing step, and is of a thickness so as to be fully removed during the removing step.

22. (original) The semiconductor device of claim 14 wherein the photoresist layer is of a thickness less than or equal to about 500 Å.

23. (original) The semiconductor device of claim 14 wherein removing the photoresist layer and the exposed region of the photosensitive layer comprises developing the photoresist layer and the exposed region with a developer.

24. (original) The semiconductor device of claim 23 wherein the developer comprises tetra-methyl-ammonium-hydroxide (TMAH).

25. (original) The semiconductor device of claim 24 wherein the developer removes the photoresist layer and the exposed region of the photosensitive layer contemporaneously.

26. (original) The semiconductor device of claim 14 wherein the photoresist layer protects regions of the photosensitive layer, other than the region above the circuit element, from exposure during the exposing step.